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10/552,046

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EXAMINER

KUSUMAKAR, KAREN M

ART UNIT

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2829

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/552,046	Applicant(s) CHEN ET AL.	
	Examiner KAREN M. KUSUMAKAR	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 and 4-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 August 2008 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Status of Claims

1. As of the amendment filed 8/20/08, no claims have been added, claims 2-3 have been canceled, and claims 1, 5, 8-10, 12-13 have been amended. Therefore, claims 1, 4-21 remain pending, with claims 1, 10, and 17 being independent.

Drawings

2. The drawings were received on 8/20/08. These drawings are accepted.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram in view of Hoffman et al. (US Patent No. 6,737,750 B1 and Hoffman hereinafter).

5. As to claim 1, Akram discloses:

a ball grid array package (Fig. 2) comprising a base IC structure, the base IC structure comprising: a base substrate (substrate 14, Fig. 2) having a first base substrate face (the upper surface of substrate 14, Fig. 2), a second base substrate face opposite to the first base substrate face (the lower surface of substrate 14, Fig.

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2), **a base substrate opening extending between the first base substrate face and the second base substrate face** (the opening between the left and right substrate 14 as shown in Fig. 2), **and a base conductor** (the interface between the substrate 14 and the bond wires must be some kind of conductor/metal/electrode in order to transmit signals as shown in Fig. 2); **a first semiconductor chip** (IC chip 12, Fig. 2), **comprising a first chip face** (the upper surface of IC chip 12, Fig. 2), **a second chip face opposite to the first chip face** (the lower surface of IC chip 12, Fig. 2), **and first bond pads disposed over the base opening** (the interfaces between the IC chip 12 and the bond wires must be some kind of conductor/metal/electrode, which serve as bond pads, in order to transmit signals as shown in Fig. 2); **and a first plurality of wires disposed to pass through the substrate base opening and electrically connecting the first bond pads to the base conductor** (the bond wires between the left and right substrate 114 as shown in Fig. 2) **[claim 1]**;

a secondary IC structure, comprising: a secondary substrate (the middle substrate 114, Fig. 2) **having a first secondary substrate face** (the upper surface of the middle substrate 114 as shown in Fig. 2), **a second secondary substrate face opposite to the first secondary substrate face** (the lower surface of the middle substrate 114 as shown in Fig. 2), **a secondary opening extending between the first secondary substrate face and the second secondary substrate face** (the opening between the left and right middle substrate 114 as shown in Fig. 2), **and a secondary conductor** (the interfaces between the middle substrate 114 and the bond wires must be some kind of conductor/metal/electrode in order to transmit signals as shown in Fig.

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2), a **second semiconductor chip** (the middle IC chip 112, Fig. 2), **comprising a second chip face** (the upper surface of the middle IC chip 112 as shown in Fig. 2), a **second chip face opposite to said second chip face** (the lower surface of the middle IC chip 112 as shown in Fig. 2), and **second bond pads disposed over the secondary opening** (the interfaces between the middle IC chip 112 and the bond wires must be some kind of conductor/metal/electrode, which serve as bond pads, in order to transmit signals as shown in Fig. 2); and a **second plurality of wires electrically connecting the second bond pads to the secondary conductor through the secondary opening** (the bond wires between the left and right middle substrate 114 as shown in Fig. 2); and a **first encapsulant filling the secondary opening around the second plurality of wires and covering the second secondary substrate face** (grease 22, Fig. 2)

although Akram discloses substantial features of the claimed invention, it fails to disclose:

Where the base substrate further comprises a plurality of vias extending between the first base substrate face and the second base substrate face; the base conductor extends through the vias; and the base substrate further comprises a layer of solder mask disposed on portions of the first and second chip faces.

Nonetheless, these features are well known in the art and would have been an obvious modification of the device disclosed by Akram, as evidenced by Hoffman.

Hoffman discloses:

where the base substrate (substrate 10, Fig. 1) **further comprises a plurality of vias** (vias 13, Fig. 1) **extending between the first base substrate face** (the upper surface of substrate 10 as shown in Fig. 1) **and the second base substrate face** (the lower surface of substrate 10 as shown in Fig. 1); **the base conductor extends through the vias** (conductive circuit patterns 11a and 11b, Fig. 1); **and the base substrate further comprises a layer of solder mask disposed on portions of the first and second chip faces** (col. 3, lines 62-67).

Given the teaching of Hoffman, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Akram by employing the well known or conventional features of vias and solder mask at the claimed locations, such as disclosed by Hoffman, in order to improve heat spreading capabilities while also prove for greater routing capacity and higher levels of IC electrical performance.

Akram discloses substantial features of the claimed invention and further discloses:

The secondary IC structure is mounted on the base IC structure (Fig. 2), **and further comprising "ball array" connecting the secondary IC structure to the base IC structure** (ball array 132, Fig. 2).

However, Akram fails to disclose:

The ball array being a plurality of wires.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the device disclosed by Akram, as evidenced by Hoffman.

Hoffman discloses:

The ball array being a plurality of wires (conductive wires 20, Fig. 1).

Given the teaching of Hoffman, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Akram by employing the well known or conventional features of wires, such as disclosed by Hoffman, in order to cost-effective connect the structures electrically.

6. As to claims 5, Akram in view of Hoffman also discloses:

molding compound encapsulating at least portions of the base IC structure and the secondary IC structure (grease 22, Akram, Fig. 2).

7. As to claim 6, Akram in view of Hoffman discloses a substantial features of the claimed invention (see paragraphs above), and further discloses:

where the molding compound (grease 22, Fig. 2) **encapsulates “ball array”** (ball array 132, Fig. 2).

However, Akram fails to disclose:

the ball array being plurality of wires.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the device disclosed by Akram, as evidenced by Hoffman.

Hoffman discloses:

the ball array being plurality of wires (conductive wires 20, Fig. 2).

Given the teaching of Akram, a person having ordinary skills in the art at the time of invention would have readily recognized the desirability and advantages of modifying Akram by employing the well known or conventional features of wires, such as disclosed by Hoffman, in order to cost-effective connect the structure electrically.

8. As to claim 7, although Akram in view of Hoffman discloses substantial features of the claimed invention, it fails to disclose:

where the first secondary chip face is free of the molding compound.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the device disclosed by Akram in view of Hoffman, as evidenced by Akram.

Akram discloses:

where “the upper surface of the chip” (inactive surface 52, in Fig. 9) is free of the molding compound (grease 22, Fig. 9).

Given the teaching of Akram, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Akram in view of Hoffman by employing the well known of conventional features of freeing a surface of the chip from the molding compound, such as disclosed by Akram, in order to make direct contact with the protective shell that serves as a die-attach, a heat sink, and a container for holding the molding compound.

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9. As to claim 8, Akram discloses substantial features of the claimed invention, and further discloses:

at least one additional of the secondary IC structure (the top IC chip 112 and the top substrate 114, Fig. 2) **mounted over the first secondary chip face** (the upper surface of the middle chip 112 as shown in Fig. 2).

However, Akram fails to disclose:

respective wires connecting a conductive portion of the at least one additional secondary IC structure to the base IC structure.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the device disclosed by Akram, as evidenced by Hoffman.

Hoffman discloses:

respective wires (conductive wires 20, Fig. 1) **connecting a conductive portion** (bond pad 16c, Fig. 3) **of “the secondary IC structure”** (second die 16 serve as the secondary IC structure, Fig. 1) **to the base IC structure** (substrate 10 and first die 12, Fig. 1).

Given the teaching of Hoffman, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Akram by employing the well known or conventional features of wires, such as disclosed by Hoffman, in order to cost-effective connect the additional structures electrically.

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10. As to claim 9 Akram in view of Hoffman disclose **a thermal dissipation element disposed over the first secondary chip face** (protective shell 34, Akram, Fig. 2; col. 4, lines 27-34; the characteristics of protective shell 24 also apply to protective shell 34).

11. As to claims 10-12, Akram discloses substantial features of the claimed invention (see paragraphs above)), and further discloses:

a method of assembling a ball grid array package, comprising: providing a base IC structure, comprising a base substrate (substrate 14, Fig. 2) **and a first semiconductor chip mounted on the base substrate in a die-down configuration** (IC chip 12, Fig. 2); **linking the bond pads of the base chip** (the interface between the IC chip 12 and the bond wires must be some kind of conductor/metal/electrode, which serve as bond pads, in order to transmit signals as shown in Fig. 2) **to the base substrate using the first plurality of wires** (the bond wires between the left and right substrate 14 as shown in Fig. 2); **providing a first secondary IC structure, comprising a secondary substrate** (the middle substrate 114, Fig. 2) **and a second semiconductor chip mounted on said second substrate in a die-down configuration** (the middle IC chip 112, Fig. 2); **mounting the first secondary IC structure to said base IC structure** (Fig. 2); **electrically connecting a conductive portion of the secondary IC structure** (the interfaces between the ball array 132 and the middle substrate 114 must be some kind of conductor/metal/electrode in order to transmit signals as shown in Fig. 2) **to a conductive portion of the base IC structure** (the interfaces between the ball array 132 and the substrate 14 must be some kind of

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conductor/metal/electrode in order to transmit signals as shown in Fig. 2) **using at least a “ball array”** (ball array 132, Fig. 2), **and encapsulating the base IC structure and the first secondary IC structure, including first plurality of wires and “ball array”** (grease 22 and protective shells 24 and 34, Fig. 2) **[claim 10];**

where the encapsulating step comprises encapsulating the first secondary IC structure (grease 22, Fig. 2) **and subsequently encapsulating the base IC structure and the first secondary IC structure, together with the first plurality of wires and “ball array”** (protective shell 34, Fig. 2) **[claim 11];**

providing a second secondary IC structure, comprising a secondary substrate (the top substrate 114, Fig. 2) **and a semiconductor chip mounted on the secondary substrate in a die-down configuration** (the top chip 112, Fig. 2); **encapsulating the second secondary IC structure** (grease 22, Fig. 2), **such that encapsulant forms a substantially planar surface on the underside of the secondary IC structure** (the grease 22 between the top substrate 114 and the middle substrate 114 has an upper and lower planar surface as shown in Fig. 2); **mounting the substantially planar surface of the encapsulant to the first secondary IC structure** (the lower planar surface touches the middle substrate 114 as shown in Fig. 2); **electrically connecting** (ball array 132, Fig. 2) **a conductive portion of the second secondary IC structure** (the interfaces between the top substrate 114 and the ball array 132 must be some kind of conductor/metal/electrode in order to transmit signals as shown in Fig. 2) **to a conductive portion of at least one of the base IC structure and the first secondary IC structure** (the interfaces between the

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ball array 132 and the middle substrate 114 must be some kind of conductor/metal/electrode in order to transmit signals as shown in Fig. 2); **and connecting the second secondary IC structure to at least one of the base IC structure and the first secondary IC structure using “ball array”** (the top ball array 132, Fig. 2) **[claim 12]**.

However, Akram fails to disclose:

the ball array being plurality of wires.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Akram, as evidenced by Hoffman.

Hoffman discloses:

the ball array being plurality of wires (conductive wires 20, Fig. 1).

Given the teaching of Hoffman, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Akram by employing the well known or conventional features of wires, such as disclosed by Hoffman, in order to cost-effective connect the structures electrically.

12. As to claims 13-15, Akram also discloses:

encapsulating at least part of the base IC structure and the secondary IC structure (grease 22, Fig. 2) **[claim 13]**;

encapsulating at least part of the base IC structure and the first secondary IC structure and the second secondary IC structure (grease 22, Fig. 2) **[claim 14]**;

attaching solder balls to the base IC structure (the bottom ball array 132, Fig. 2) **[claim 15]**.

13. As to claim 16, although Akram discloses substantial features of the claimed invention (see paragraphs above), it fails to disclose:

singulation of the entire BGA structure.

Nonetheless, this feature is well known in the art and would have been an obvious modification of the method disclosed by Akram, as evidenced by Hoffman.

Hoffman discloses:

singulation of the entire BGA structure (col. 13, lines 9-15).

Given the teaching of Hoffman, a person having ordinary skills in the art at the time of the invention would have readily recognized the desirability and advantages of modifying Akram by employing the well know or conventional features of singulation, such as disclosed by Hoffman, in order to sever the substrate strip into a plurality of semiconductor packages.

14. As to claim 17-20, the combination of Akram and Hoffman applied to claims 1-9 above also applies.

15. As to claim 21, Akram in view of Hoffman also discloses:

where the first chip (IC chip 12, Fig. 2) and the second IC chip are substantially the same size (the middle IC chip 112, Akram, Fig. 2).

Response to Arguments

16. Applicant's arguments filed 8/20/08 have been fully considered but they are not persuasive. Applicant makes three arguments:

- a. Replacing the solder balls with wires would require a redesign of the entire structure, as the solder balls are supporting the second substrate.
- b. Solder balls and wire bonds are two different technologies that are not easily interchangeable
- c. Hoffman does not teach the third plurality of wires extending from the secondary substrate to the base substrate.

17. Examiner respectfully disagrees for the following reasons:

As to argument a), examiner maintains that connections can be made between wires, vias, balls, or any combination thereof. Hoffman and Akram both show that it is known in the art to use wires, vias, and balls (see figures 2 of both references). By way of example only, if one were to replace just one solder ball on each side of the substrate opening (Akram figure 2) with wires, the substrate would still be supported and no redesign would be necessary.

As to argument b), examiner respectfully disagrees with this argument. Both technologies are used for connection purposes, and they are interchangeable. Whether or not it is easily done is moot. What is important is if there is a distinct advantage to interchanging them. Things that are not easy are done all the time so long as the advantage of it outweighs the difficulty of it.

As to argument c), the Hoffman reference shows foot 14f (figure 2) connected to the ball 15 through the via 13 (col. 6:45-47). As stated above, various connection types are known and can be used interchangeably. Hoffman teaches a connection to the substrate through the foot. It could have just as easily been a wire connection. Or, if one would interpret the claim more broadly, the third plurality of wires can be considered wire 16b, which connects the secondary substrate 14 to the base substrate 10 via chip 16a and wire 20. Still yet another way to read on this limitation is Akram inherently has wires or traces in the secondary substrate 114 (figure 2) that connect the wire of the secondary substrate to the ball 132, which connects to the base substrate 14.

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

19. Any response to this Office Action should be faxed to (571) 273-8300 or mailed to:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-Delivered responses should be brought to:

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22313

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAREN M. KUSUMAKAR whose telephone number is (571) 270-3520. The examiner can normally be reached on Mon - Thurs 7:30a - 5:00p EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/K. M. K./
Examiner, Art Unit 2829
11/21/2008

/Ha T. Nguyen/
Supervisory Patent Examiner, Art Unit 2829